CLAIMS

What is claimed is:

1. A transceiver for processing high data rate serial data, comprising:

phase-locked loop circuitry further including selectable coarse loop PLL and selectable fine loop PLL circuits, the selectable coarse loop PLL for producing a coarse loop synchronized oscillation signal based on a reference clock, the coarse loop synchronized oscillation signal having a specified degree of accuracy relative to a received serial data rate and the selectable fine loop PLL for adjusting the coarse loop synchronized oscillation signal to further synchronize with the received high data rate serial data; and

mode determination logic coupled to produce mode switching signals to selectively switch the selectable coarse loop PLL and selectable fine loop PLL into and out of coupling according to defined operational logic within the mode determination logic.

2. The transceiver of claim 1 wherein the mode determination logic produces the mode switching signals responsive to one of an automatic mode, a sample mode, and a receive mode of operation.

3. The transceiver of claim 2 wherein the mode determination logic, when in the automatic mode of operation, further operates according to an initial (coarse) calibration mode of operation and a final (fine) calibration mode of operation.

4. The transceiver of claim 3 wherein the mode determination logic, when in the initial calibration mode, selectively de-couples the selectable fine loop PLL and couples the selectable coarse loop PLL.

5. The transceiver of claim 4 wherein the mode determination logic selectively couples the selectable fine loop PLL after a specified period.

6. The transceiver of claim 5 wherein the mode determination logic selectively de-couples the selectable coarse loop PLL.

7. The transceiver of claim 4 wherein the mode determination logic selectively couples the selectable fine loop PLL after determining that a received clock derived from an oscillation corresponding to a coarse error signal is within the specified degree of accuracy relative to the received serial data rate.

8. The transceiver of claim 7 wherein the mode determination logic selectively de-couples the selectable coarse loop PLL.

9. The transceiver of claim 3 wherein the automatic mode of operation is a default mode of operation.

10. The transceiver of claim 9 wherein the mode determination logic operates according to the automatic mode of operation responsive to a mode selection signal received from an external source.

11. The transceiver of claim 1 wherein the mode determination logic, when in the sample mode of operation, selectively de-couples the selectable fine loop PLL and couples the selectable coarse loop PLL as long as the transceiver is in the sample mode of operation.

12. The transceiver of claim 3 wherein the mode determination logic prompts the phase-locked loop circuitry

to lock to a local reference for data sampling operations responsive to the mode selection signal received from the external source.

13. The transceiver of claim 3 wherein the mode determination logic prompts the phase-locked loop circuitry to lock to the received serial data rate responsive to the mode selection signal received from the external source.

14. A high data rate transceiver, comprising:

a first programmable receive PMA module coupled to produce a first serial data;

a first clock and data recovery (CDR) coupled to receive the first serial data, the first CDR producing a first recovered clock in a first CDR receive mode of operation and producing a first sample clock in a first CDR sample mode of operation;

a second programmable receive PMA module coupled to produce a second serial data;

a second CDR coupled to receive the second serial data, the second CDR producing a second recovered clock in the first CDR receive mode of operation and producing a second sample clock in a second CDR sample mode of operation;

the first and second CDRs each further including selectable fine loop and coarse loop PLLs; and

programmable logic fabric further comprising:

mode determination logic for determining, for each of the first and second CDRs, the CDR receive mode of operation; and

mode switching logic for generating and providing mode switching signals to the first and second CDRs to select which of the selectable fine loop PLL and course loop PLL are selectively coupled within each CDR to provide a corresponding receive or sample clock.

15. The high data rate transceiver of claim 14 wherein the mode determination logic determines to operate in an automatic mode as a default mode of operation.

16. The high data rate transceiver of claim 15 wherein the mode determination logic, as a part of automatic mode, places at least one of the first and second CDRs in an initial (coarse) calibration mode for one of a specified period or until determining that a coarse loop synchronization oscillation signal as produced by selectable coarse loop PLL is within a specified degree of accuracy relative to a received serial data rate.

17. The high data rate transceiver of claim 16 wherein the mode determination logic, as a part of automatic mode, places at least one of the first and second CDRs in a final (receive) mode subsequent to placing the at least one of the first and second CDRs in the initial (coarse) calibration mode.

18. The high data rate transceiver of claim 15 wherein the mode determination logic determines to operate in a sample mode of operation based upon mode control signals received from an external source.

19. The high data rate transceiver of claim 18 wherein the mode determination logic generates mode switching signals to the at least one of the first and second CDRs to de-couple fine loop synchronization circuitry and to couple coarse loop synchronization circuitry.

20. A transceiver for processing high data rate serial data, comprising:

transceiver circuitry for transmitting and receiving the high data rate serial data;

phase-locked loop circuitry further including a selectable coarse loop PLL and a selectable fine loop PLL, wherein:

the selectable coarse loop PLL for producing a coarse error signal reflecting a difference between a reference signal and a coarse loop feedback signal; and

the selectable fine loop PLL for producing a fine loop error adjustment signal based upon a difference in a recovered clock and the high data rate serial data;

a loop filter for producing an error signal based on at least one of the fine loop error adjustment signal from a fine loop charge pump and the coarse error signal from a coarse loop charge pump;

a controlled oscillation module for producing a receiver clock in the form of an oscillating signal based on the error signal produced by the loop filter;

a divider for dividing the oscillating signal to produce the recovered clock to a phase detector;

a selectable coarse loop selection switch coupled between the coarse loop charge pump and the loop filter;

coarse loop logic circuitry for providing control commands to couple the selectable coarse loop PLL to the loop filter based upon one of a sample mode signal or a detected difference between a reference clock and the coarse loop feedback signal;

a selectable fine loop selection switch coupled between the fine loop charge pump and the loop filter; and

mode determination logic external to the fine loop PLL and coarse loop PLL coupled to produce mode switching signals to selectively switch the selectable coarse loop PLL and selectable fine loop PLL into and out of coupling according to defined operational logic within the mode determination logic.

21. The transceiver of claim 20 wherein the mode switching signals comprise a sample mode signal and a logical opposite of the sample mode signal.

22. The transceiver of claim 20 wherein the mode determination logic produces the mode switching signals responsive to one of an externally specified automatic mode, a sample mode, and a receive mode of operation.

23. The transceiver of claim 22 wherein the transceiver, when in the automatic mode of operation further operates according to an initial (coarse) calibration mode of operation and a final (fine) calibration mode of operation.

24. The transceiver of claim 23 wherein the mode determination logic, when in the initial calibration mode, produces a fine loop calibration signal to de-couple the selectable fine loop PLL and a coarse loop calibration signal to couple the selectable coarse loop PLL.

25. The transceiver of claim 24 wherein the mode determination logic selectively couples the selectable fine loop PLL after a specified period.

26. The transceiver of claim 25 wherein the mode determination logic selectively de-couples the selectable coarse loop PLL after the specified period.

27. The transceiver of claim 24 wherein the mode determination logic selectively couples the selectable fine loop PLL after determining that a recovered clock derived from an oscillation signal corresponding to the coarse error signal as produced by the selectable coarse loop PLL is within the specified degree of accuracy relative to the received high data rate serial data.

28. The transceiver of claim 27 wherein the mode determination logic selectively de-couples the selectable coarse loop PLL.

29. The transceiver of claim 23 wherein the automatic mode of operation is a default mode of operation.

30. The transceiver of claim 23 wherein the error signal produced by the loop filter is a voltage signal and further wherein the controlled oscillation module produces the corresponding oscillation characterized by an oscillation frequency that is a function of a magnitude of the voltage signal.

31. The transceiver of claim 22 wherein the mode determination logic, when in a sample mode of operation, selectively de-couples the selectable fine loop PLL and couples the selectable coarse loop PLL as long as the transceiver is in the sample mode of operation.

32. The transceiver of claim 23 wherein the mode determination logic prompts the phase-locked loop circuitry to lock to a local reference for data sampling operations responsive to a mode selection signal received from an external source.

33. The transceiver of claim 23 wherein the mode determination logic prompts the phase-locked loop circuitry to lock to the received high data rate serial data responsive to the mode selection signal received from the external source.

34. A multi-gigabit transceiver for processing high data rate serial data, comprising:

transceiver circuitry for transmitting and receiving the high data rate serial data;

phase-locked loop (PLL) means for producing a first clock based upon a reference signal and a second clock based upon received high data rate serial data; and

logic for selecting between the first clock and the second clock, the logic producing mode switching signals to prompt the phase-locked loop means to produce one of the first and second clocks.

35. The transceiver of claim 34 wherein the mode switching signals comprise at least one of a sample mode signal and a logical opposite of the sample mode signal.

36. The transceiver of claim 34 wherein the PLL means comprises fine loop circuitry and coarse loop circuitry for producing the first and second clocks responsive to the mode switching signals.

37. A method for producing a reference clock, comprising:

receiving a specified mode of operation;

generating mode switching signals to selectively couple at least one of coarse loop PLL and fine loop PLL according to a specified mode of operation;

wherein the mode switching signals de-couple the fine loop PLL and produce, solely from the coarse loop PLL, a first clock based upon a reference clock based in a first (sample) mode of operation;

wherein, the mode switching signals de-couple the coarse loop PLL and couple the fine loop PLL and produce a second clock based upon received serial data in a second (lock to received data) mode of operation; and

wherein the mode switching signals initially couple the coarse loop PLL and de-couple the fine loop PLL and, after one of a specified period or condition, de-couple the coarse loop PLL and couple the fine loop PLL, all in a third (automatic) mode of operation.

38. The method of claim 37 wherein the mode switching signals are generated to de-couple the fine loop PLL and to couple the coarse loop PLL as long as the specified mode is the sample mode of operation.

39. Automated Test Equipment (ATE) circuitry, comprising:

input/output circuitry for receiving communication signals and for producing high data rate inbound serial data;

phase-locked loop (PLL) circuitry coupled to receive the high data rate inbound serial data wherein the PLL circuitry operates in a sample mode based upon a mode control signal; and

mode control logic to generate the mode control signal to prompt the PLL circuitry to operate in the sample mode.

40. The ATE circuitry of claim 39 wherein the ATE circuitry is formed at least in part within programmable logic of a field programmable gate array.

41. The ATE circuitry of claim 39 wherein the ATE circuitry is formed at least in part within programmable functions of a multi-gigabit transceiver.